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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,371	09/16/2003	Katsunori Yamazaki	116573	9410

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EXAMINER	
XIAO, KE	
ART UNIT	**PAPER NUMBER**
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.**	**Applicant(s)**	
	10/662,371	YAMAZAKI, KATSUNORI	
	Examiner	**Art Unit**	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2 and 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (JP 06-027899) in view of Inoue (US 6,342,881).

Regarding **Claims 1 and 7**, Yamazaki teaches an electro-optical device including a plurality of scanning lines and a plurality of data lines, which are wired to cross the scanning lines (Yamazaki, Fig. 5 elements X1-X6 and Y1-Y6), comprising:

an electrode, which is wired to cross the data lines and is capacitively coupled with the data lines (Yamazaki, Fig. 5 elements Y2 and Y5);

a feedback logic circuit that includes an input terminal and adjusts an input signal supplied to the input terminal to produce an output signal, the input signal being a signal generated at the electrode biased to a predetermined level, the output signal being a pulse whose pulse amplitude corresponds to a magnitude relationship of the signal generated at the electrode and the predetermined level (Yamazaki, Fig. 5, element 531 and reference voltages V1 and V4); and

logic circuits that selectively adjust a signal supplied to each scanning line by a predetermined amount, in part, upon the output value produced by the feedback logic circuit (Yamazaki, Fig. 5 elements 532, 533, V5).

Yamazaki fails to teach that the feedback logic circuit includes an inversion circuit that inverts an input signal and produces a binary pulse width modulated output signal as claimed. Inoue teaches a LCD display device which inverts scan line and data line signals as well as pulse width modulated output signal based on an input signal (Inoue, Fig. 10 and 22 polarity inversion and Fig. 14 binary pulse width modulation). It would have been obvious to one of ordinary skill in the art at the time of the invention to add the inversion logic circuit of Inoue to the display device of Yamazaki in order to allow for polarity inversion to further eliminate crosstalk between electrodes. It would also have been obvious to one of ordinary skill in the art at the time of the invention to replace the amplitude modulation of Yamazaki with the binary pulse width modulation of Inoue in order to obviate the use of the voltage divider and reduce the drive voltage levels provided to the pixel elements. Additionally such a combination would require two predetermined adjustment levels one for positive adjustment and one for negative adjustments depending on the polarity of the signals. Inoue also teaches that the biased level is higher or lower than an input threshold voltage of the inversion logic circuit depending on a polarity of a datum to display (Inoue, Fig. 10 and 22 per pixel polarity inversion and overdriving of the polarity signals).

Regarding independent **Claim 2**, Yamazaki teaches an electro-optical device (Yamazaki, Fig. 5) including:

a plurality of scanning lines (Yamazaki, Fig. 5 elements Y1-Y6);

a scanning line driving circuit that supplies to each of the scanning lines a scanning signal which is set to be at a selection level and a non-selection level corresponding to a selection period and a non-selection period of each scanning line (Yamazaki, Fig. 9);

a plurality of data lines which are wired to cross the scanning lines (Yamazaki, Fig. 5 elements X1-X6);

a data line driving circuit that supplies to each of the data lines a data signal on the basis of display data (Yamazaki, Fig. 5 element 11); and

pixels provided in portions where the scanning lines cross the data lines and driven on the basis of the scanning signals and the data signals (Yamazaki, Figs. 5 and 9 elements X and Y),

the electro-optical device comprising:

an electrode, which is wired to cross the data lines and is capacitively coupled with the data lines (Yamazaki, Fig. 5 elements Y2 and Y5);

a feedback logic circuit that includes an input terminal and adjusts an input signal supplied to the input terminal to produce an output signal, the input signal being a signal generated at the electrode biased to a predetermined level, the output signal being a pulse whose pulse amplitude corresponds to a magnitude relationship of the

signal generated at the electrode and the predetermined level (Yamazaki, Fig. 5, element 531 and reference voltages V1 and V4); and

logic circuits that selectively adjust a signal supplied to each scanning line a predetermined amount based, in part, upon the output value produced by the inversion logic circuit (Yamazaki, Fig. 5 elements 532, 533, V1' and V2').

Yamazaki fails to teach that the feedback logic circuit includes an inversion circuit that inverts an input signal and produces a binary pulse width modulated output signal as claimed. Inoue teaches a LCD display device which inverts scan line and data line signals as well as pulse width modulated output data signals based on an input signal (Inoue, Fig. 10 polarity inversion and Fig. 14 binary pulse width modulation). It would have been obvious to one of ordinary skill in the art at the time of the invention to add the inversion logic circuit of Inoue to the display device of Yamazaki in order to allow for polarity inversion to further eliminate crosstalk between electrodes. It would also have been obvious to one of ordinary skill in the art at the time of the invention to replace the amplitude modulation of Yamazaki with the binary pulse width modulation of Inoue in order to obviate the use of the voltage divider and reduce the drive voltage levels provided to the pixel elements. Additionally such a combination would require two predetermined adjustment levels one for positive adjustment and one for negative adjustments depending on the polarity of the signals. Inoue also teaches that the biased level is higher or lower than an input threshold voltage of the inversion logic

circuit depending on a polarity of a datum to display (Inoue, Fig. 10 and 22 per pixel polarity inversion and overdriving of the polarity signals).

Regarding **Claim 4**, Yamazaki further teaches the logic circuits not adjusting the signal supplied to each scanning line at an early state of the selection period to the selection level (Yamazaki, Fig. 5 feedback loops always have a delay therefore it can be considered not an early state).

Regarding independent **Claim 5**, Yamazaki teaches a method of driving an electro-optical device including a plurality of scanning lines (Yamazaki, Fig. 5 element Y1-Y6), a scanning line driving circuit that supplies to each of the scanning lines a scanning signal which is set to be at a selection level and a non-selection level corresponding to a selection period and a non-selection period of each scanning line (Yamazaki, Fig. 9), a plurality of data lines which are wired to cross the scanning lines, a data line driving circuit that supplies to each of the data lines a data signal on the basis of display data (Yamazaki, Fig. 5 element X1-X6), and pixels provided in portions where the scanning lines cross the data lines and driven on the basis of the scanning signals and the data signals (Yamazaki, Fig. 5, X and Y), the method comprising:

wiring an electrode to cross the data lines and is capacitively coupling the electrode with the data lines (Yamazaki, Fig. 5 elements Y2 and Y5);

supplying an input signal to an input terminal of an feedback logic circuit, the input signal being a signal generated at the electrode biased to a predetermined level (Yamazaki, Fig. 5, element 531, reference V1 and V4);

adjusting the input signal to produce an output signal, the output signal being a pulse whose amplitude corresponds to a magnitude relationship of the signal generated at the electrode and the predetermined level; and

selectively adjusting a signal supplied to each scanning line by one of two predetermined amounts based, in part, upon the output value (Yamazaki, Fig. 5 elements 532, 533, V1' and V2').

Yamazaki fails to teach that the feedback logic circuit includes an inversion circuit that inverts an input signal and produces a binary pulse width modulated output signal as claimed. Inoue teaches a LCD display device which inverts scan line and data line signals as well as pulse width modulated output signal based on an input signal (Inoue, Fig. 10 polarity inversion and Fig. 14 binary pulse width modulation). It would have been obvious to one of ordinary skill in the art at the time of the invention to add the inversion logic circuit of Inoue to the display device of Yamazaki in order to allow for polarity inversion to further eliminate crosstalk between electrodes. It would also have been obvious to one of ordinary skill in the art at the time of the invention to replace the amplitude modulation of Yamazaki with the binary pulse width modulation of Inoue in order to obviate the use of the voltage divider and reduce the drive voltage levels provided to the pixel elements. Additionally such a combination would require two predetermined adjustment levels one for positive adjustment and one for negative adjustments depending on the polarity of the signals. Inoue also teaches that the biased level is higher or lower than an input threshold voltage of the inversion logic

circuit depending on a polarity of a datum to display (Inoue, Fig. 10 and 22 per pixel polarity inversion and overdriving of the polarity signals).

Regarding independent **Claim 6**, Yamazaki teaches a circuit for driving an electro-optical device (Yamazaki, Fig. 5) including:

a plurality of scanning lines (Yamazaki, Fig. 5 elements X1-X6 and Y1-Y6);

a scanning line driving circuit that supplies to each of the scanning lines a scanning signal which is set to be at a selection level and a non-selection level corresponding to a selection period and a non-selection period of each scanning line (Yamazaki, Fig. 5 element 12);

a plurality of data lines which are wired to cross the scanning lines (Yamazaki, Fig. 5 elements X1-X6);

a data line driving circuit that supplies to each of the data lines a data signal on the basis of display data, and pixels provided in portions where the scanning lines cross the data lines and driven on the basis of the scanning signals and the data signals (Yamazaki, Fig. 5 element 11).

the circuit comprising an electrode, which is wired to cross the data lines and is capacitively coupled with the data lines (Yamazaki, Fig. 5 elements Y2 and Y5);

an input terminal, wherein an input signal supplied to the input terminal being adjusted to produce an output signal, the input signal being a signal generated at the electrode biased to a predetermined level, the output signal being a pulse whose pulse amplitude corresponds to a magnitude relationship of the signal generated at the

electrode and the predetermined level (Yamazaki, Fig. 5, element 531 and reference voltages V1 and V4); and

the circuit selectively adjusts a signal supplied to each scanning line b one of two predetermined amounts based, in part, upon the output value (Yamazaki, Fig. 5 elements 532, 533, V1' and V2').

Yamazaki fails to teach that the feedback logic circuit includes an inversion circuit that inverts an input signal and produces a binary pulse width modulated output signal as claimed. Inoue teaches a LCD display device which inverts scan line and data line signals as well as pulse width modulated output signal based on an input signal (Inoue, Fig. 10 polarity inversion and Fig. 14 binary pulse width modulation). It would have been obvious to one of ordinary skill in the art at the time of the invention to add the inversion logic circuit of Inoue to the display device of Yamazaki in order to allow for polarity inversion to further eliminate crosstalk between electrodes. It would also have been obvious to one of ordinary skill in the art at the time of the invention to replace the amplitude modulation of Yamazaki with the binary pulse width modulation of Inoue in order to obviate the use of the voltage divider and reduce the drive voltage levels provided to the pixel elements. Additionally such a combination would require two predetermined adjustment levels one for positive adjustment and one for negative adjustments depending on the polarity of the signals. Inoue also teaches that the biased level is higher or lower than an input threshold voltage of the inversion logic

circuit depending on a polarity of a datum to display (Inoue, Fig. 10 and 22 per pixel polarity inversion and overdriving of the polarity signals).

Regarding **Claims 8-11**, Yamazaki further teaches that the output value generated by the inversion logic circuit is high if a signal level generated in the electrode is lower than the predetermined level and low if a signal level generated in the electrode is higher than the predetermined level (Yamazaki, Paragraphs [0044-0049] depending on the value generated by the electrode Yamazaki balances the final adjustment voltage which satisfies the claim language).

Response to Arguments

Applicant's arguments filed January 11th, 2008 have been fully considered but they are not persuasive.

The applicant argues that Yamazaki fails to teach a signal generated at the electrode is biased to a predetermined level that is higher or lower than a input threshold voltage of the inversion logic circuit depending on a polarity of a datum to display. Specifically the applicant argues that the instant application discloses the signal generated at the electrode is compared with the input threshold voltage of an inversion logic circuit and then is biased to a predetermined level that is higher or lower than the input threshold. The examiner respectfully disagrees. The claim doesn't recite any limitations regarding comparisons and doesn't define exactly what input threshold voltage is for the inversion logic circuit. The examiner therefore broadly interprets the

input threshold voltage to be any activation voltage of the logic circuit, and since the inversion circuit has overdrive capability the voltage is inherently biased to either greater than or less than the input threshold voltage.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Ke Xiao/
Examiner, Art Unit 2629